REMARKS/ARGUMENTS

Claims 14 - 16 and 21 - 24 are pending.

Claims 14 - 16, 21, and 22 were rejected under 35 U.S.C. Section 102 for allegedly being anticipated by Hayano.

The present invention relates to inspection in semiconductor processing. An aspect of the invention as recited in amended claim 14 is "presenting a graphical indication of a size distribution of the particles or defects in each of the regions." Fig. 13 in the instant application shows an illustrative embodiment of this aspect of the invention, discussed on page 65, lines 3 - 20. A graph is presented to a user, showing on one axis particle size and on the other axis number of particles. Regions are identified with different colored bars. Fig. 14 shows an alternative embodiment, specification on page 65, line 21 to page 66, line 5.

Hayano show in Figs. 15A - 15C a reticle 1 having been partitioned into cells. *Col. 15, lines 55 - 60.* Each cell is associated with the "largest" defect among the defects in that cell. As explained in col. 16, lines 10 - 14, when a plurality of defects are detected in a cell, "a defect having a larger sample value of the detection signal V is used as a representative sample value of the cell."

Hayano discuss in Fig. 16A classifying defects and presenting a display which is "ranked A, B, or C in correspondence with the sample value of a detection signal of the maximum defect in the corresponding cell" *Col. 16, lines 24 - 26.* The ranks are shown in a window (20, Fig. 16A), where for each cell size (e.g., 5 mm^2 cell size, 0.1 mm^2 cell size) the number of defects of each rank is shown.

By contrast, the present invention recites presenting a graph of "size distribution of the particles or defects in each of the regions." *Claim 14.* Hayano does not show "size distribution" but rather teaches ranking based on signal strength of a detection signal. For at least this reason, the Section 102 rejection of claim 14 in view of the amendment made to claim 14 is believed to be overcome.

An aspect of the invention as recited in appended claim 23 is dividing the regions "according to a plurality of pattern densities formed on the dies." Fig. 11 shows an illustrative

embodiment of this aspect of the invention, which is described on page 62, lines 3 to 18. The figure shows an example of a microprocessor chip having different circuit areas, such as memory and data I/O circuits. The regions are divided according to each circuit area.

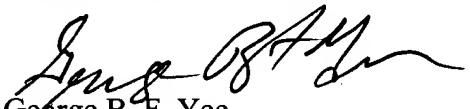
It appears from a review of Hayano that this aspect of the present invention is not taught. It is earnestly believed therefore that Hayano does not anticipate this aspect of the invention.

CONCLUSION

In view of the foregoing, all claims now pending in this Application are believed to be in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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